Full-Chip CDM Analysis: Is Static Simulation Enough?

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Objective and Significance

Due to complexity and cost of developing today's integrated circuits, it has become increasingly important to perform full chip simulations to find ESD weak points. In this poster, charged device model (CDM) simulations are reviewed. Such CDM events are characterized by fast high-current pulses that lead to high voltages being generated within the IC under test, with the highest voltage overshoot generated early in the pulse.

To improve understanding and verification of ICs before manufacturing, a static approach to CDM verification and analysis is explored. In the absence of full-chip transient circuit simulation, considered computationally prohibitive, approximations can be made to account for transient effects. Through the use of these methods in static simulation, potentials failures have been successfully found.

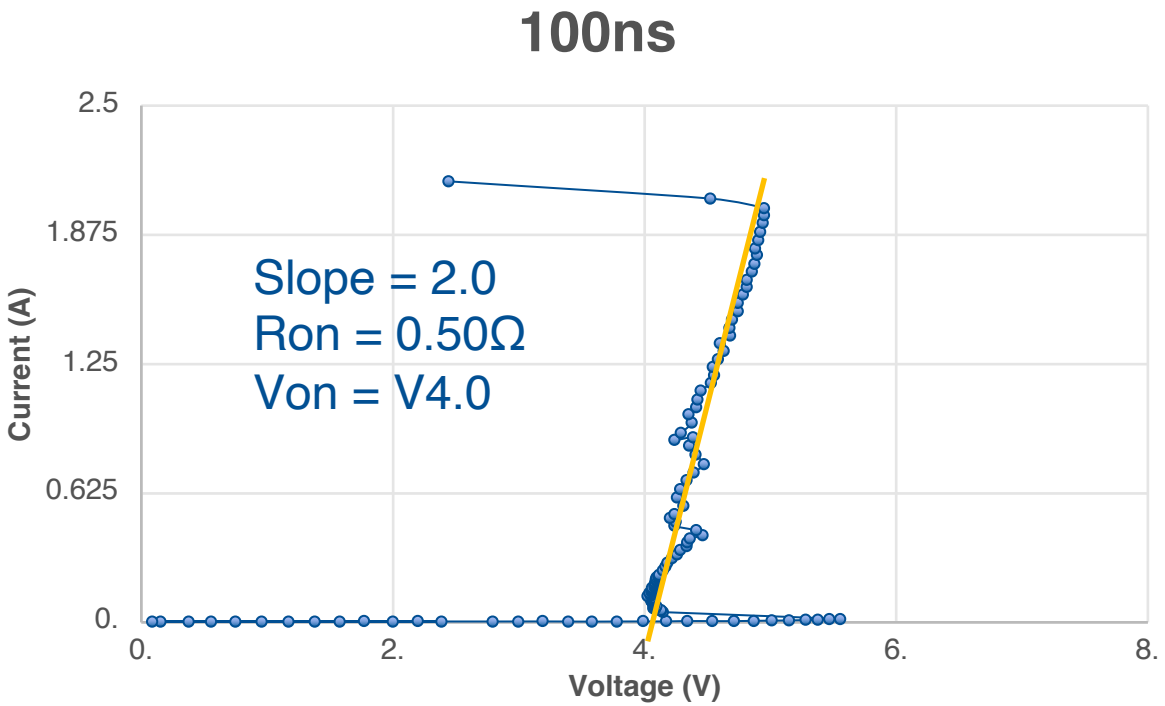
Static simulations with some iterative capabilities along with transient approximations are proposed as the optimum solution for full chip verification.

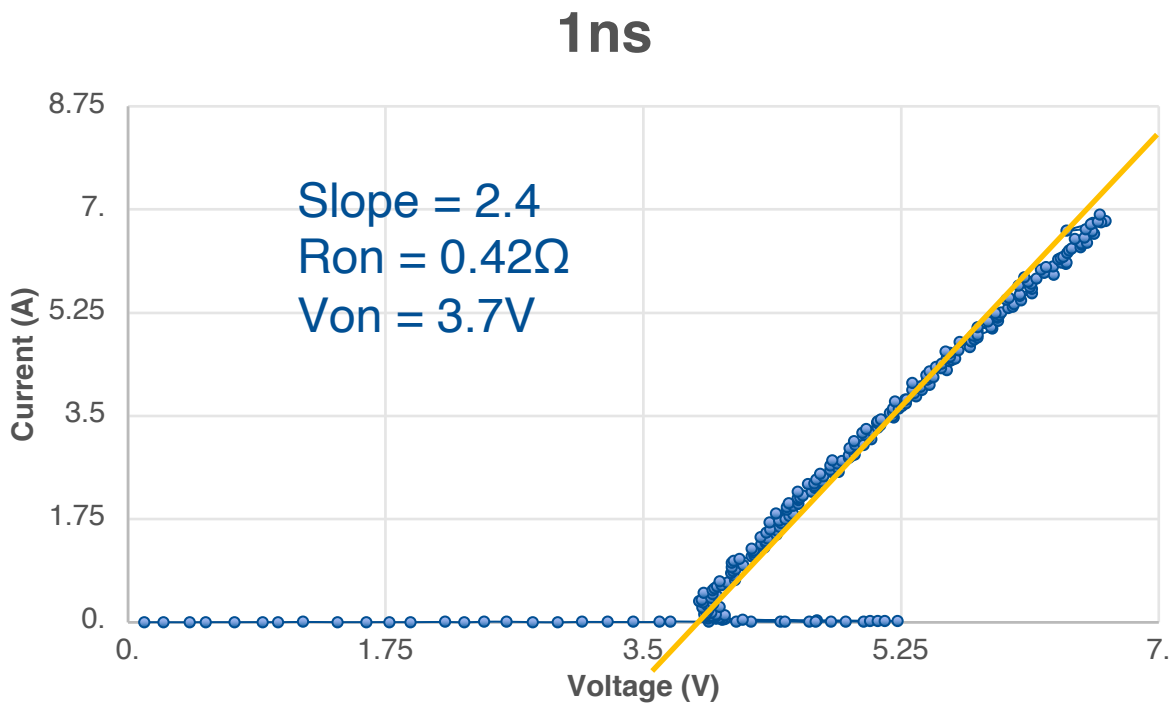
Biography

- Career
  - ON Semi - ESD design intern, March 2008
  - ON Semi - ESD discrete device & process designer, 2009 - 2017
  - Samsung Electronics - Full chip ESD verification, 2017 - present
- Education
  - B.S.E in electrical engineering in 2009, Arizona State University
  - M.S.E in electrical engineering in 2015, Arizona State University
- Life
  - Wife of 14 years and 8 great kids
  - Serving my church, missions, and those around me
  - Exploring, camping, learning all the things Korea has to offer

Static Device Behavior

- Determining static device behavior for ESD snapback devices:

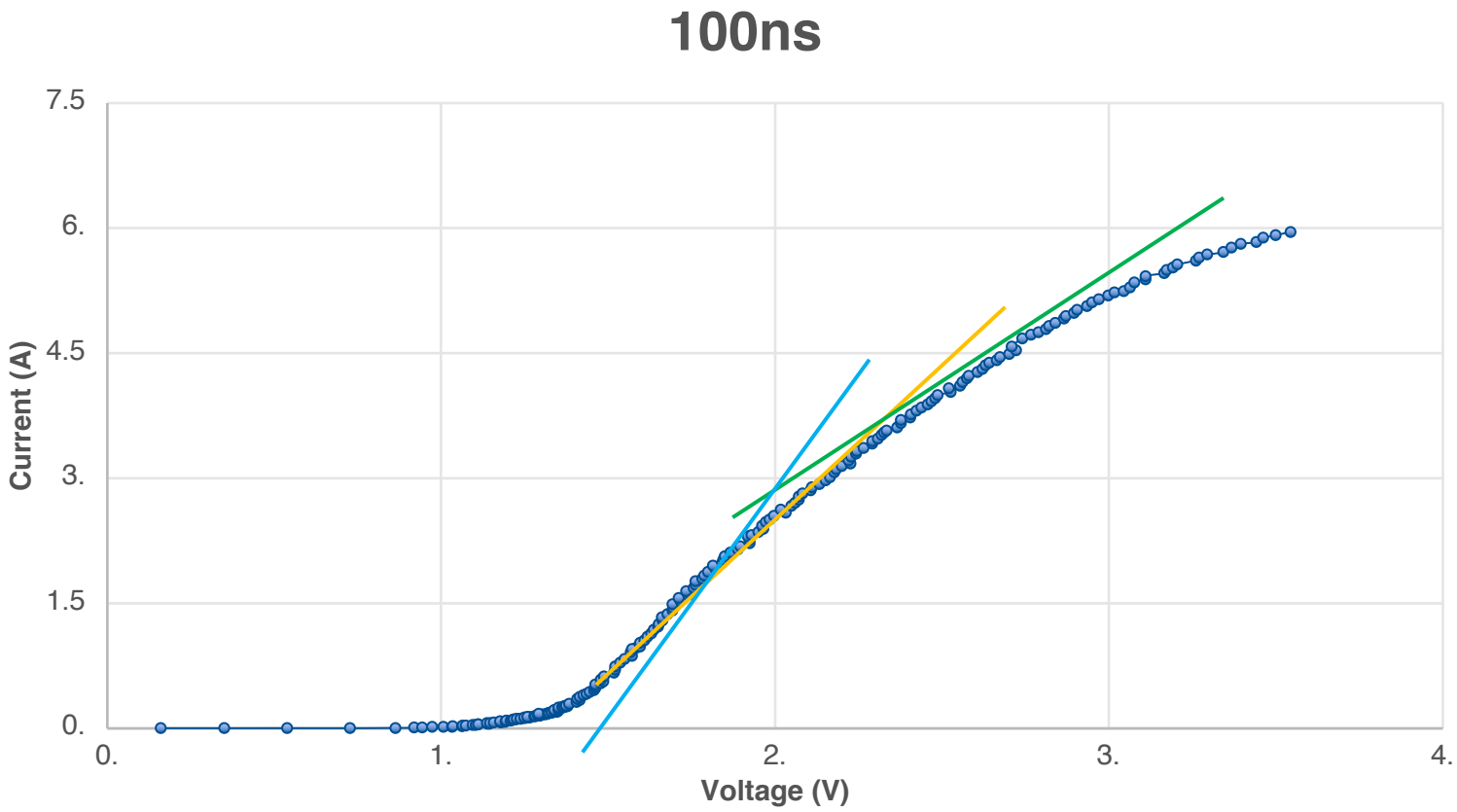




- 1ns VF-TLP values were used
  - 100ns TLP values will capture all failures, but may introduce false errors
  - 8% variation Von and 16% variation Ron between time scales

Static Device Behavior

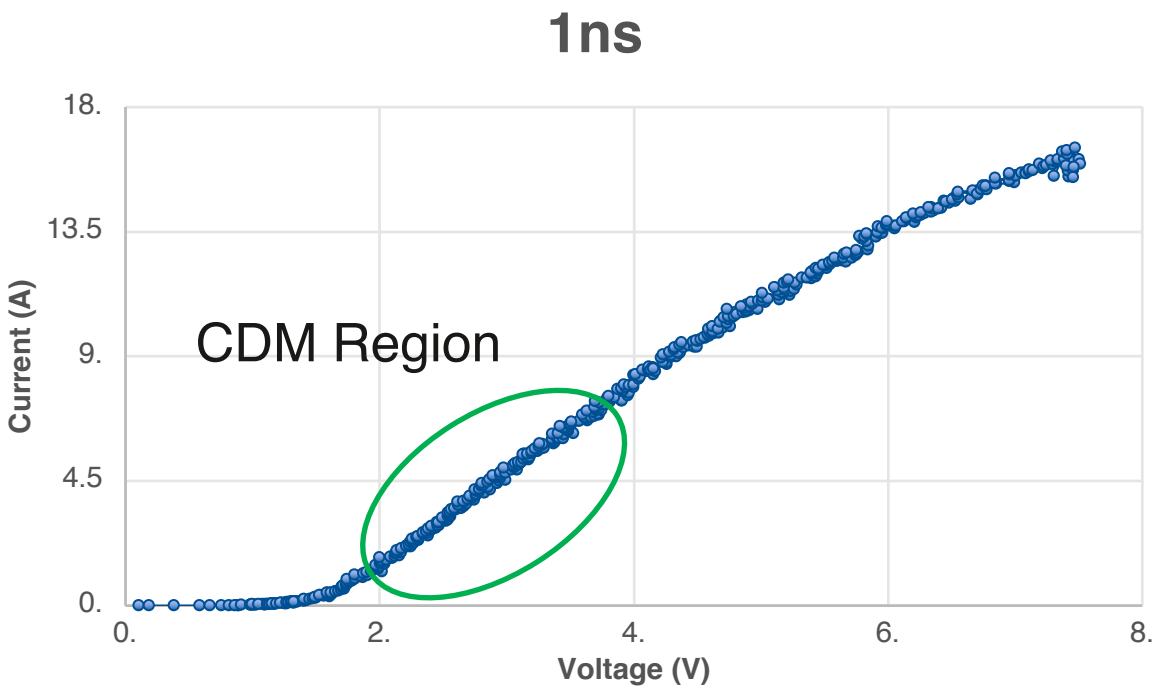
- Determining static device behavior for ESD Diodes:

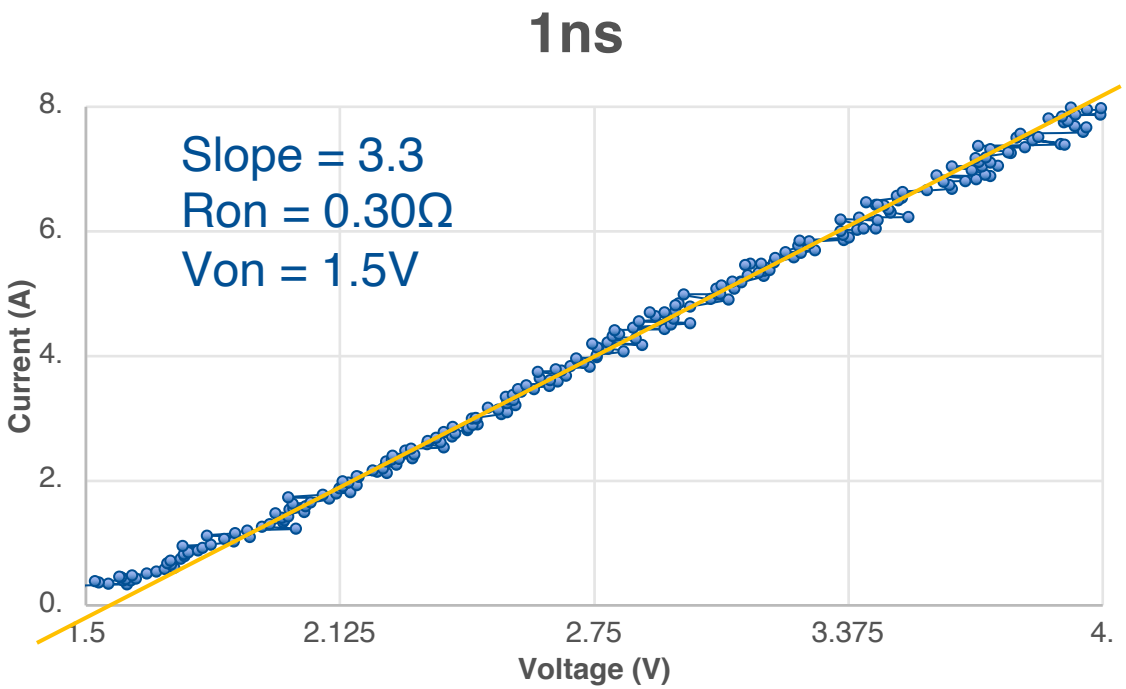


- 100ns diode varying slope is problematic for choosing Ron and Von
  - Pseudo-linear region can be chosen, but which one

Static Device Behavior

- Determining static device behavior for ESD Diodes:

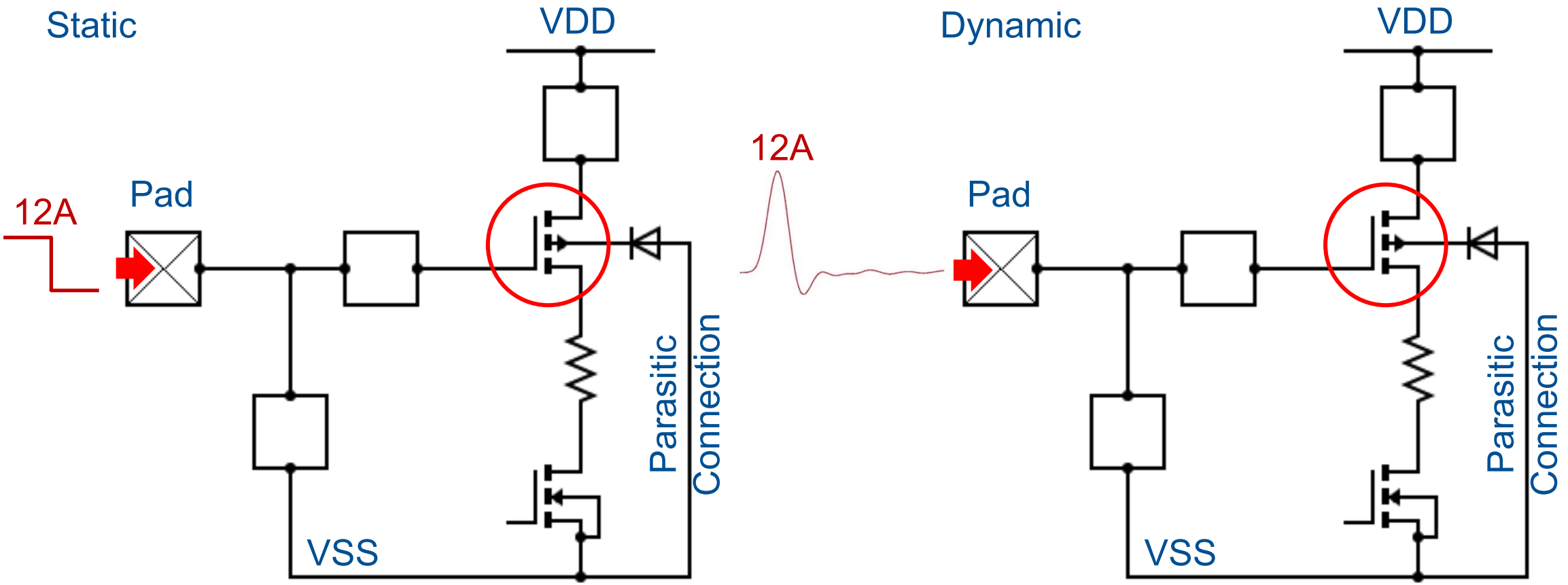




- Current range for 250V and 500V CDM provides a linear region for parameter extraction

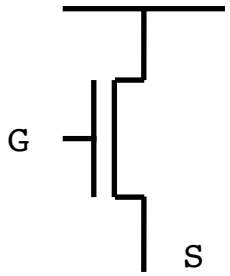
Static Versus Dynamic

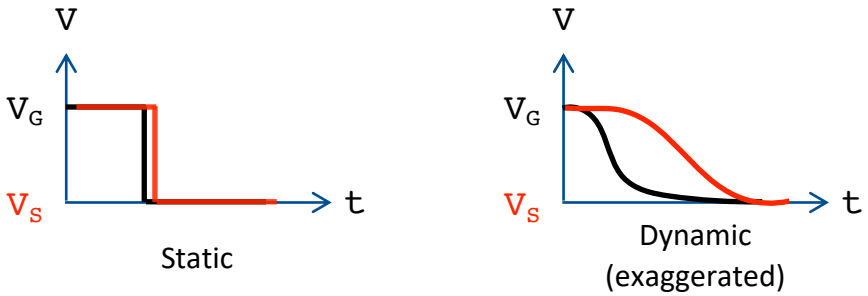
- Difference in peak current and propagated voltage
- Static simulation creates higher stress condition



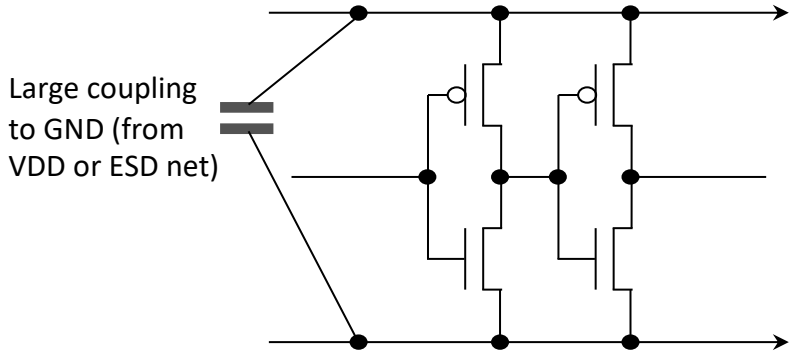
Static Vs. Dynamic

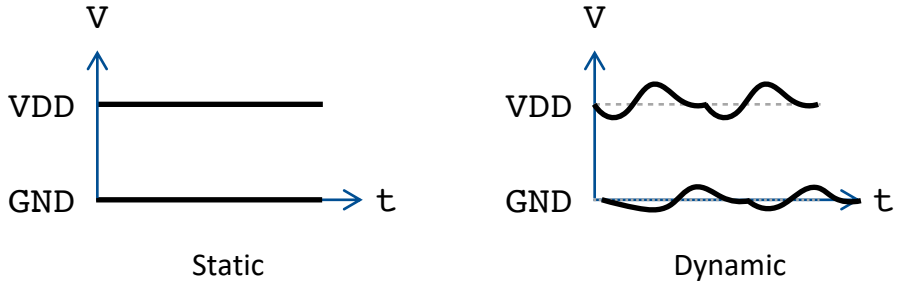
- Two examples where static analysis is pessimistic





- Static delta-V > dynamic delta-V

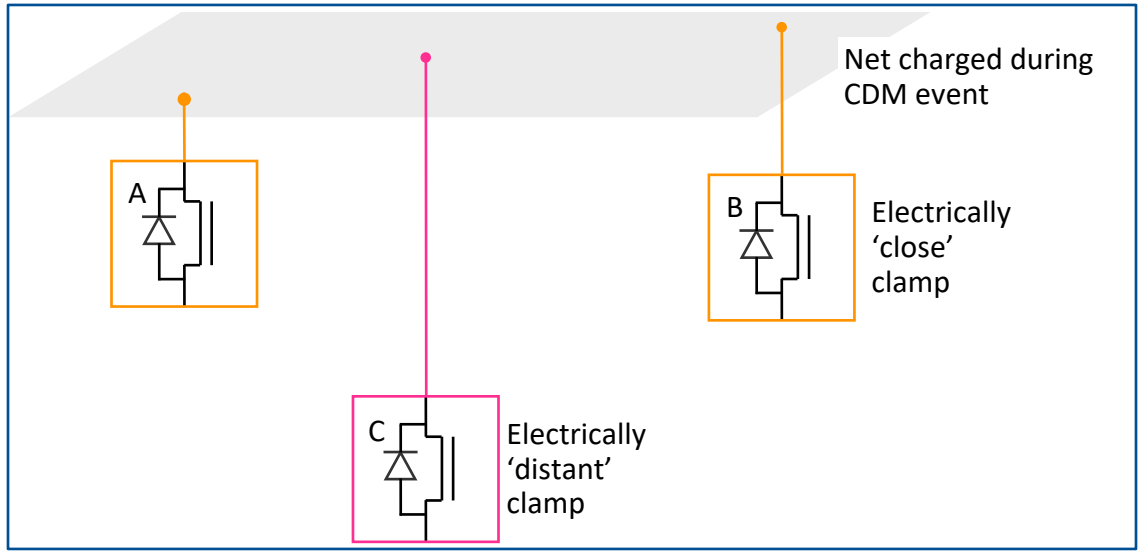


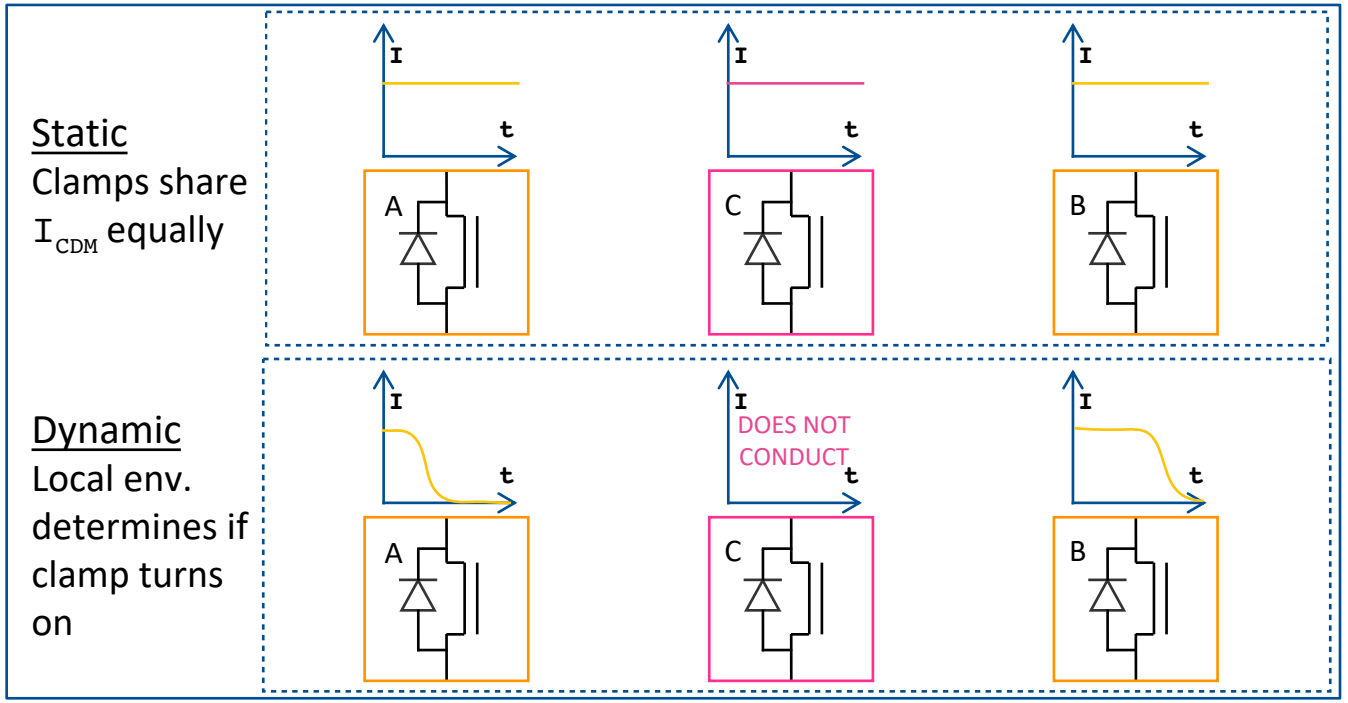


- Static delta-V > dynamic delta-V

Transient ESD Device Behavior

- Turn-On latency

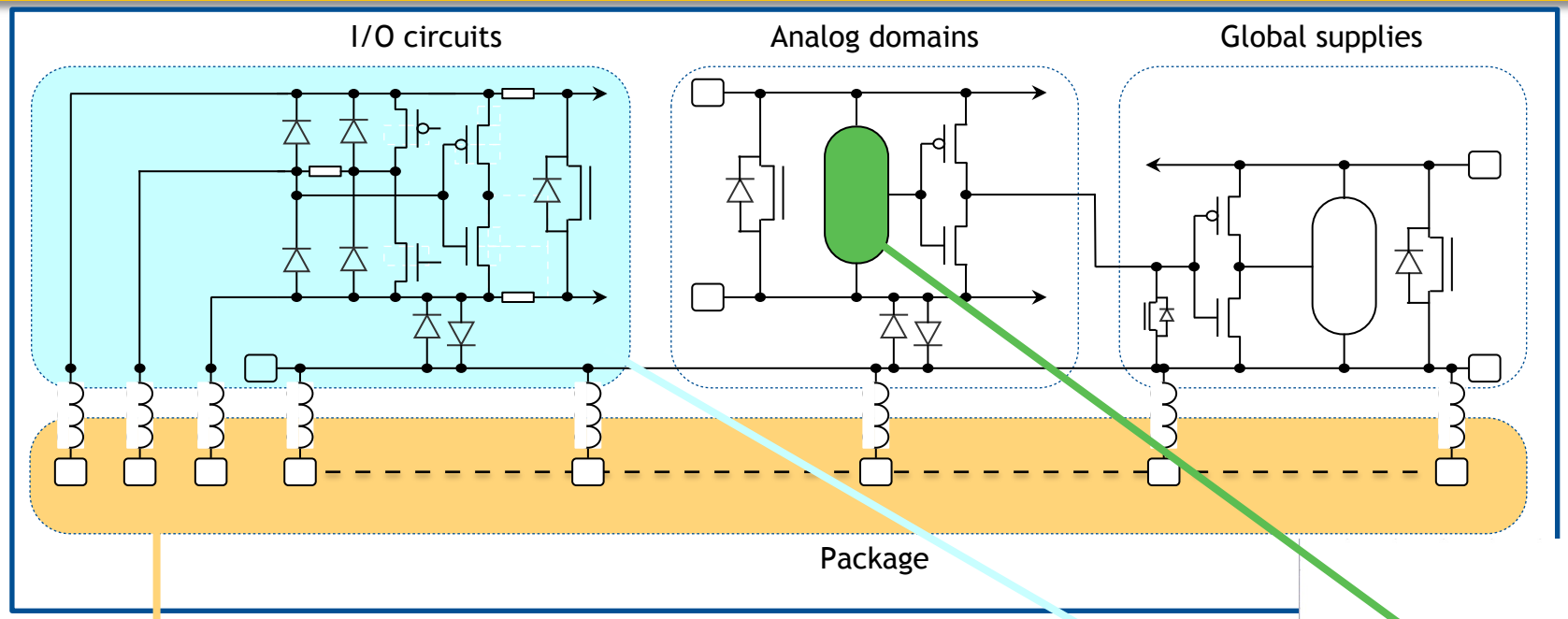




- ESRA uses proprietary algorithms to reduce false violations
- Globally static
- Locally pseudo-dynamic

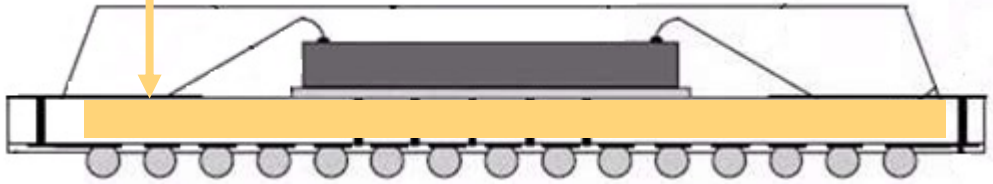
- Here, ESRA models pseudo-dynamic state
  - Static simulation assumes all devices are conducting
  - Electrically distant devices are on, but see lower voltage due to voltage drop ofofinterconnect

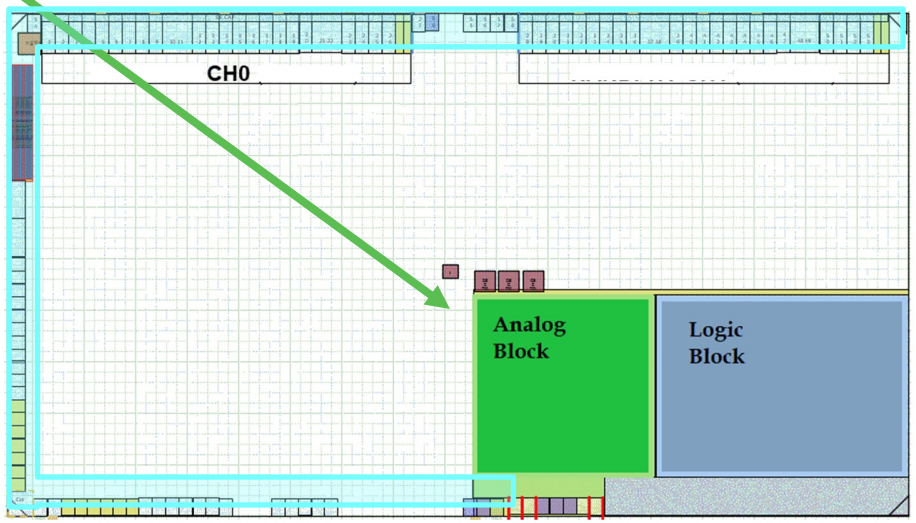
Bond Wire Inductance



Package-contained net R included
Bond-wire related L effect included

BGA Wire bond example

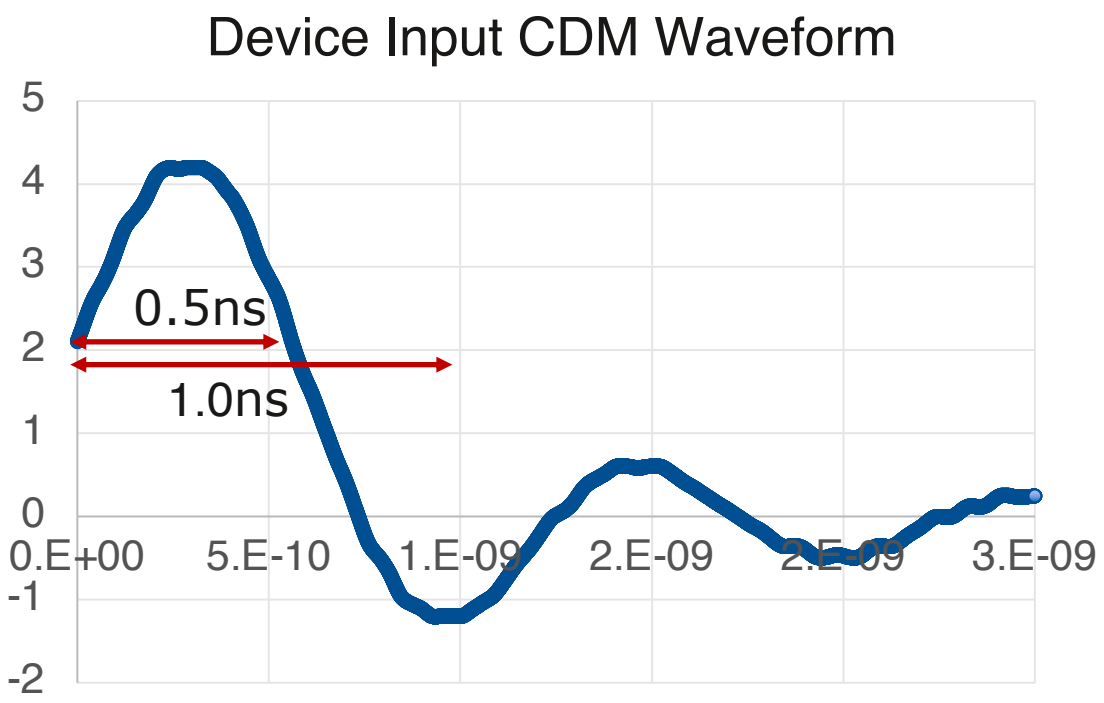


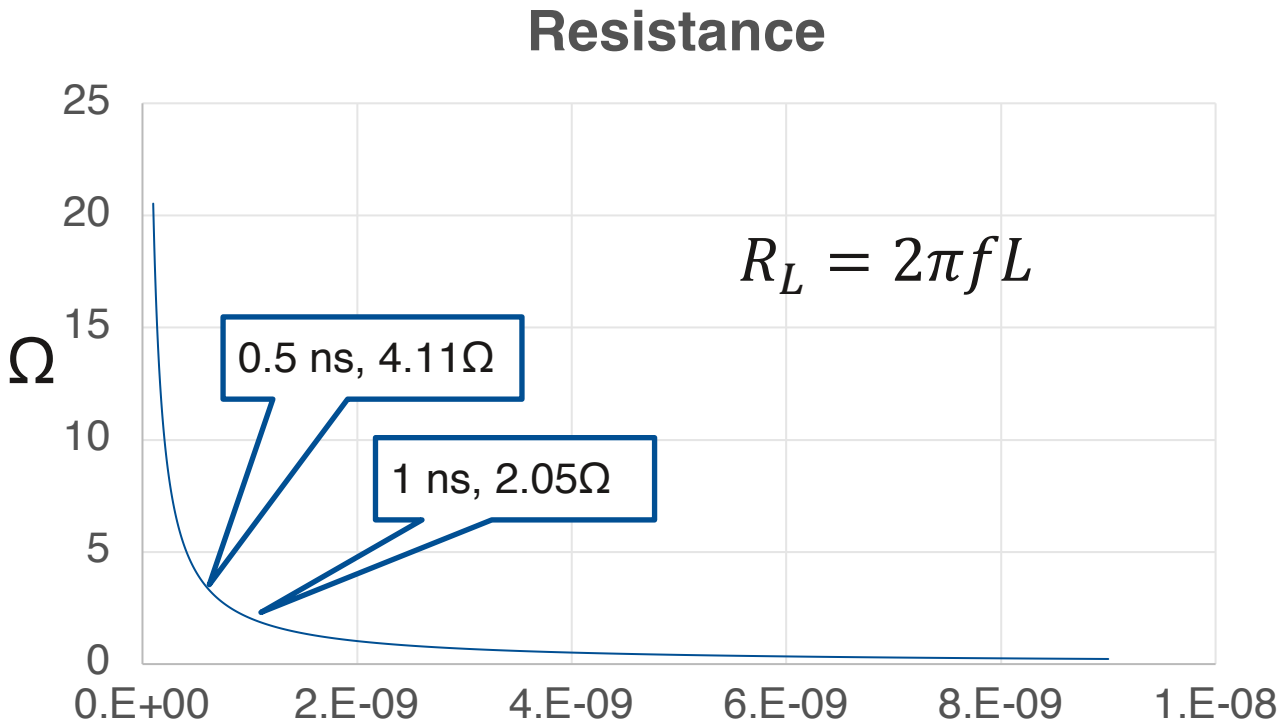


Bond Wire Inductance Approximation

- Calculated resistance value can compensate for bond wire inductance in static simulation.
- CDM peak pulse duration can be used for frequency.

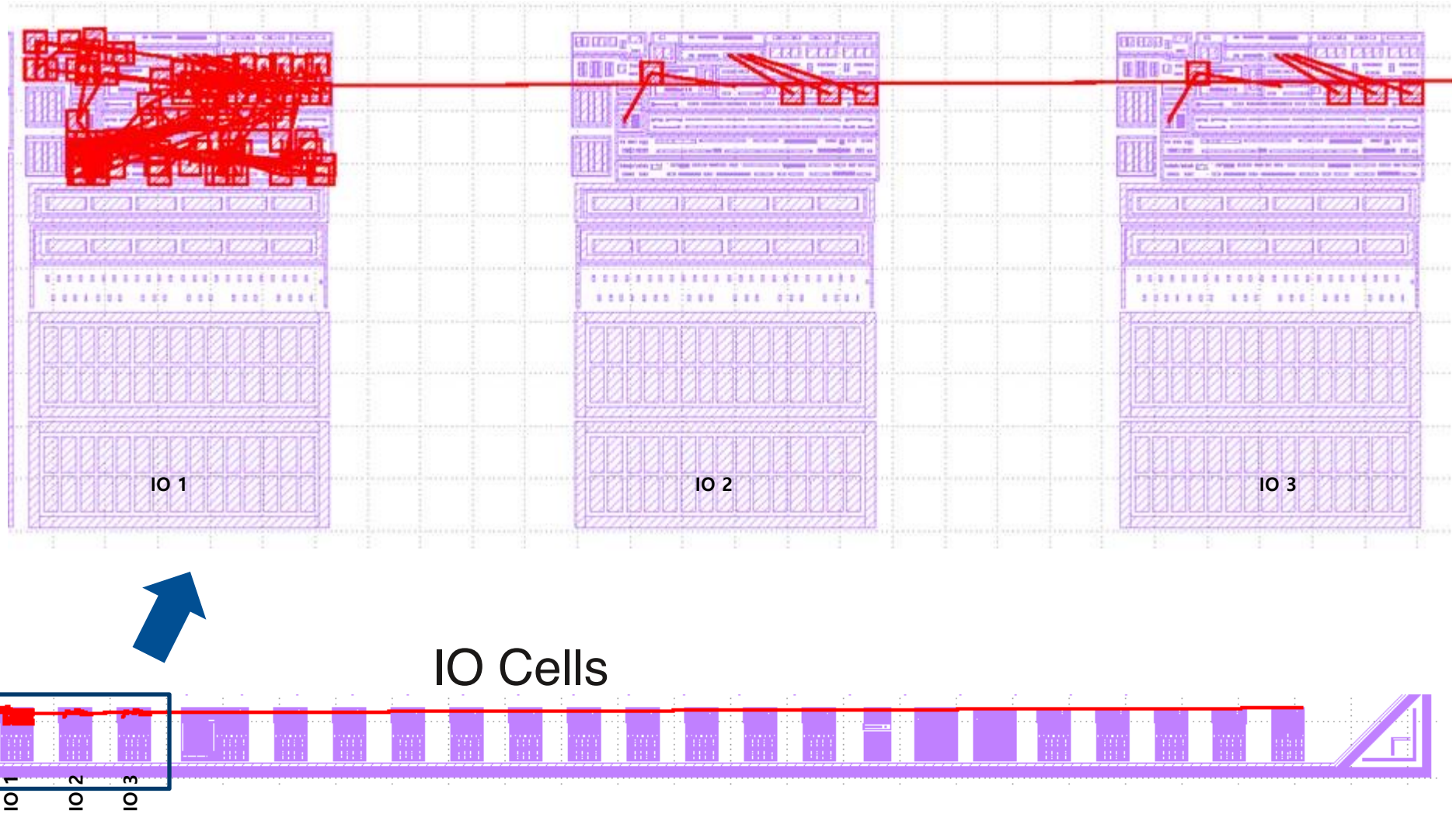
$$L = \frac{\mu_0}{2\pi} * l\left[ln\left(\frac{2l}{r}\right) - 0.75\right]$$



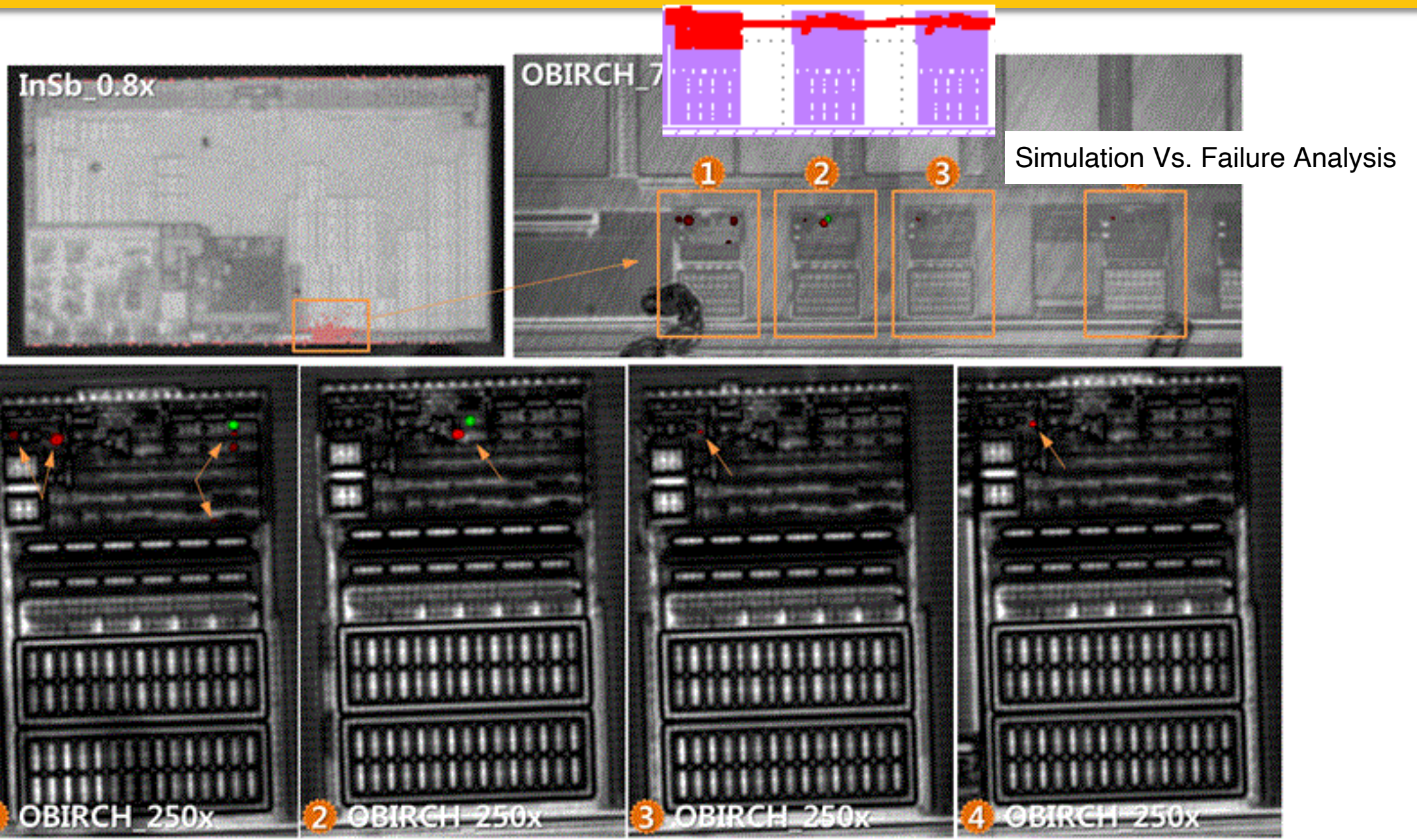


Static Simulation Analysis

- Static simulation results



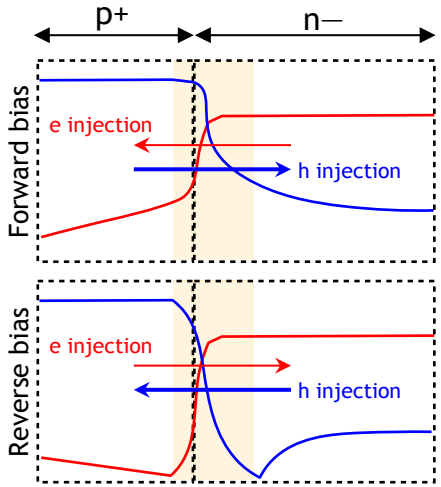
Failure Analysis Results for the same case



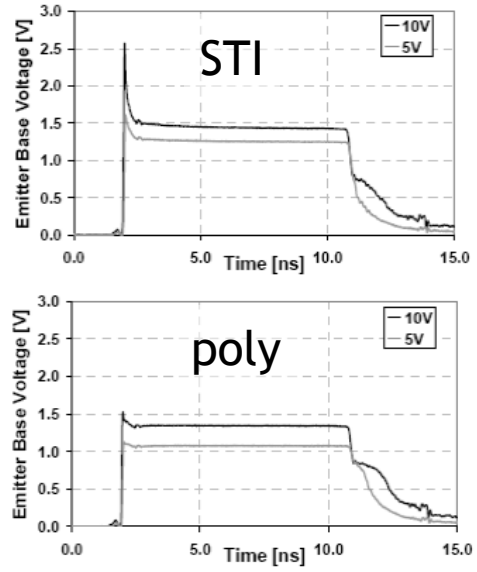
Other Transient ESD Device Behaviors

- Voltage overshoot is not captured in static simulation
  - In static simulation:
    - All devices have constant resistance
    - Devices are on or off with no transition state

Diode forward and reverse recovery



- Charge redistribution creates a transient voltage overshoot during turn-on



- CMOS Diode Analysis
- Some devices have greater susceptibility to overshoot.

[Man07] J.-R. Manouvrier, P. Fonteneau, C.-A. Legrand, P. Nouet, F. Azaïs; "Characterization of the Transient Behavior of Gated/STI Diodes and their Associated BJT in the CDM Time Domain", EOS/ESD Symposium 2007.

Additional Transient-Related Discussion Points

- Specific transient related behaviors
  - Diode and GGNMOS Gate protection
  - Switching FETs
  - Inter-rail parasitic capacitance
  - Package location of pulse
  - Integrated vs. peak power

Conclusion

- In advanced nodes with ICs that have billions of devices, dynamic simulations are a computational impossibility.
- Static simulations can take into account transient effects through approximations
- Static simulation produces a higher stress scenario that dynamic.
- Not all transient effects can be captured, but most lead to more favorable results than static simulations.

- While static simulation of full chip devices for CDM can’t capture all transient effects, it can still be used effectively to find weak and high risk areas of designs that dynamic simulation tools cannot.

Acknowledgements

- Thank you to the many people